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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/720,846	11/24/2003	Kazuo Taguchi	9319S-000578	3610

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HARNESS, DICKEY & PIERCE, P.L.C.
P.O. BOX 828
BLOOMFIELD HILLS, MI 48303

EXAMINER	
IVEY, ELIZABETH D	

ART UNIT	PAPER NUMBER
1775	

DATE MAILED: 08/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/720,846	TAGUCHI, KAZUO	
	Examiner	Art Unit	
	Elizabeth Ivey	1775	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 May 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3 and 11-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 11-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1-3 and 11-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,245610 B1 to Wang et al. in view of U.S. Patent 6,071,803 to Rutten et al.

Regarding claims 1-3 Wang discloses a substrate structure having a first conductive type substrate with at least a second conductive type (p or n-type) well region viz. pattern, having a further doped region in the well region, viz. pad. Wang further discloses a first dielectric layer with at least two plugs, viz. a conductive layer pattern, to couple with the wells (column 1 lines 38-46 and 61-67 and column 2 line 1). Wang also discloses a second dielectric, viz. insulating,

layer formed on the first dielectric layer and a metal layer formed on top of the second dielectric, viz. insulating, layer. Although Wang does not disclose the material of the top metal layer or electrical interconnection between the devices, Rutten discloses a silicon-on-insulator (SOI) semiconductor substrate structure having a support substrate with a p or n-type well region, an insulating layer on the substrate and a silicon layer, viz. single crystal silicon, grown on the insulator (column 5 lines 52-58, and 65-66 and column 6 lines 23-26, 33-46). Rutten further discloses contact trenches delineated between the devices above and below to provide electrical interconnection within the structure (column 7 lines 15-17). Because Wang discloses a structure very similar to Ruttan but lacking the electrical connection for application of an electrical potential, and because the structures are so similar it would have been obvious to a person having ordinary skill in the art at the time of the invention to utilize the electrical connection and silicon material of Ruttan in the structure of Wang in the absence of disclosure of an electrically connected structure and material disclosure by Wang.

Regarding claims 11, and 14 Wang discloses a substrate structure having a first conductive type substrate with at least a second conductive type (p or n-type) well region viz. pattern, having a further doped region in the well region, viz. pad. Wang further discloses a first dielectric layer with at least two plugs, viz. a conductive layer pattern, to couple with the wells (column 1 lines 38-46 and 61-67 and column 2 line 1). Wang also discloses a second dielectric, viz. insulating, layer formed on the first dielectric layer and a metal layer formed on top of the

second dielectric insulating layer. Although Wang does not disclose the material of the top metal layer or electrical interconnection between the devices, Rutten discloses a similar silicon-on-insulator (SOI) structure having a similar p-type or n-type support substrate with a p or n-type well region, viz. pattern, an insulating layer on the substrate and a silicon layer grown on the insulator (column 5 lines 52-58, 65-66 and column 6 lines 23-26, 33-46). Rutten further discloses contact trenches delineated between the devices above and below to provide electrical interconnection within the structure (column 7 lines 15-17). Rutten also discloses an isolation trench formed in the top silicon layer and p or n-type doping areas and a gate, which can be integrated circuit elements, in and on the silicon layer (column 7 lines 59-61, column 8 lines 18-26 and figures 1-4). Rutten also discloses an isolation trench formed in the top silicon layer and p or n-type doping areas and a gate, which can be integrated circuit elements, in and on the silicon layer (column 7 lines 59-61, column 8 lines 18-26 and figures 1-4). Because Wang discloses a structure very similar to Ruttan but lacking the electrical connection for application of an electrical potential, and because the structures are so similar it would have been obvious to a person having ordinary skill in the art at the time of the invention to utilize the electrical connection, the isolation trench and the silicon material of Ruttan in the structure of Wang in the absence of disclosure of an electrically connected structure and material disclosure by Wang.

Regarding claims 12-13 and 15-16, Wang and Rutten disclose all of the limitations of claims 11 and 14 and because the disclosed substrate exemplifies the claimed invention the disclosed well pattern could be used to control the electric potential relating to an integrated circuit element and can be used as a wiring layer and a component in a passive layer.

Response to Arguments

Examiner acknowledges applicant's amendment to claims 1, 11 and 14 and cancellation of claims 4-10 and 17 and withdraws the 112 rejections to claims 1-3.

Applicant's arguments with respect to claims 1-3 and 11-16 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Elizabeth Ivey whose telephone number is (571) 272-8432. The examiner can normally be reached on 7:00- 4:30 M-Th and 7:00-3:30 alt. Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jennifer McNeil can be reached on (571) 272-1540. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Elizabeth D. Ivey

JENNIFER C. MCNEIL
SUPERVISORY PATENT EXAMINER

8/17/06